CLAIMS:

1. An electronic circuit comprising:
- a plurality of storage elements (101 – 105) arranged for storing of data elements,
- a plurality of processing elements arranged for processing data elements stored in the plurality of storage elements,
wherein storage elements of the plurality of storage elements are further arranged to load their data elements at respective points in time of a first set of points in time, and wherein the points in time are mutually different in order to meet a maximum allowable value of the power consumption peaks.

2. An electronic circuit according to claim 1, wherein the electronic circuit further comprises:
- a clock generator arranged to generate periodic clock signals (111),
- delay elements (107, 109) arranged to generate a point in time of the first set for a respective one of the storage elements by adding respective delays to a source clock signal, wherein the respective delays are mutually different,
and wherein the frequency of the clock generator is low enough in order to ensure data integrity during processing of the data elements.

3. An electronic circuit according to claim 1, further comprising a timing circuit arranged to determine the first set of points in time in a first operating mode,
wherein the timing circuit is further arranged to determine a second set of points in time, in a second operating mode, at which respective storage elements of the plurality of storage elements load their data elements, wherein the respective points in time of the second set of points in time are essentially identical,
and wherein the timing circuit is further arranged to select an operating mode depending on a control signal (CS).

4. An electronic circuit according to claim 3, wherein the timing circuit comprises a first clock generator arranged to generate periodic clock signals (219), each to determine the respective points in time of the first set of points in time, and wherein the timing circuit further comprises a second clock generator arranged to generate periodic clock signals (217), each to determine the respective points in time of the second set of points in time.

5. An electronic circuit according to claim 4, further comprising:
- delay elements (207, 209) arranged to generate a point in time of the first set for a respective one of the storage elements by adding respective delays to a source clock signal (219), wherein the respective delays are mutually different.

6. An electronic circuit according to claim 3, wherein the timing circuit comprises a clock generator arranged to generate periodic clock signals (325), each to determine the respective points in time of either the first set of points in time or the second set of points in time, depending on the control signal (CS).

7. An electronic circuit according to claim 1, wherein the electronic circuit is a self-timed circuit, further comprising:
- a handshake channel (507) arranged for communication between storage elements of the plurality of storage elements and processing elements of the plurality of processing elements,
- delay elements (107, 109) arranged to generate a point in time of the first set for a respective one of the storage elements by adding respective delays to a request signal for loading of the data elements, wherein the delays are mutually different.

8. An electronic circuit according to claim 1, wherein the electronic circuit is a self-timed circuit, further comprising:
- handshake channels (607 – 613) arranged for communication between storage elements (601 – 605) of the plurality of storage elements and processing elements of the plurality of processing elements,
- a first handshake component (SEQ) arranged to receive a request signal, in a first operating mode, for loading of data elements and in response thereto to generate a

request signal for a respective one of the storage elements of the plurality of storage elements for loading of data elements at respective points in time of the first set of points in time.

9. An electronic circuit according to claim 8, further comprising:

- a second handshake component (PAR) arranged to receive a request signal, in a second operating mode, for loading of data elements and in response thereto to generate a request signal for a respective one of the storage elements (701 – 705) of the plurality of storage elements for loading of data elements,

wherein the request signals are generated at essentially identical points in time,

and wherein the electronic circuit is further arranged to select an operating mode depending on a control signal (CS).

10. A method of processing data elements, the method comprising:

- determining a first set of points in time, in a first operating mode, for storing data elements in respective storage elements (101 – 105) of a plurality of storage elements,

- generating output data elements each by performing respective logic operation on respective data elements,

wherein the points in time of the first set of points in time at which respective storage elements load their data elements are mutually different in order to meet a maximum allowable value of the power consumption peaks.

11. A method of processing data elements according to claim 10, further comprising:

- determining a second set of points in time, in a second operating mode, for storing data elements in respective storage elements of the plurality of storage elements, wherein the points in time of the second set of points in time at which respective storage elements load their data elements are essentially identical,

- selecting an operating mode, depending on a control signal.